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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/603,769	06/26/2003	Kei Murayama	300.1118	4072

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STAAS & HALSEY LLP
SUITE 700
1201 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

EXAMINER	
RAO, ANAND SHASHIKANT	
ART UNIT	**PAPER NUMBER**
2621	

DATE MAILED: 04/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/603,769	MURAYAMA, KEI	
	Examiner	Art Unit	
	Andy S. Rao	2621	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-12 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-12 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 3/14/05.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 3-7, 9-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Spigarelli et al., (hereinafter referred to as "Spigarelli").

Spigarelli discloses semiconductor chip mounting apparatus for mounting a semiconductor chip on a substrate by flip-chip bonding (Spigarelli: figure 2), comprising: a stage on which the substrate is carried (Spigarelli: column 8, lines 45-55), a visible light source for directly illuminating the substrate from above the stage (Spigarelli: column 12, lines 50-67), a semiconductor chip conveying means for holding from one surface said semiconductor chip comprised of silicon formed to a thickness through which visible light can pass and conveying it on said substrate carried on the stage (Spigarelli: column 10, lines 15-45), a capturing means arranged at a position facing said stage and capturing visible light passing through said semiconductor chip held by said semiconductor chip conveying means so as to capture patterns

formed on the substrate carried on said stage and said semiconductor chip (Spigarelli: column 9, lines 55-67; column 11, lines 1-10), and a positioning means for positioning said semiconductor chip on said substrate based on the patterns of said substrate and said semiconductor chip captured by said capturing means (Spigarelli: column 9, lines 45-65), as in claim 1.

Regarding claim 3, Spigarelli discloses wherein said visible light includes light of a wavelength of 660 to 760 nm (Spigarelli: column 16, lines 35-67; column 17, lines 1-55), as in the claim.

Regarding claim 4, Spigarelli discloses wherein said semiconductor chip conveying means clamps and holds said semiconductor chip at a plurality of locations (Spigarelli: column 10, lines 28-37), as in the claim.

Regarding claim 5, Spigarelli discloses wherein said semiconductor chip conveying means is provided with at least one transparent part and clamps and holds said semiconductor chip at its entire surface other than said transparent parts (Spigarelli: column 11, lines 20-50), as in the claim.

Regarding claim 6, Spigarelli discloses wherein said semiconductor chip conveying means has a transparent part through which visible light passes up to the held semiconductor chip (Spigarelli: column 11, lines 20-50), as in the claim.

Spigarelli discloses semiconductor chip mounting method for mounting a semiconductor chip on a substrate by flip-chip bonding (Spigarelli: column 26, lines 1-43) including the steps of: holding a semiconductor chip comprised of silicon formed to a thickness passing visible light by a semiconductor chip conveying means from one surface and conveying it on a substrate carried on a stage (Spigarelli: column 10, lines 15-45), directly illuminating said substrate with

visible light from above the stage (Spigarelli: column 12, lines 50-67), capturing visible light passing through said semiconductor chip by a capturing means arranged at a position facing said stage and thereby capturing patterns formed by said substrate and said semiconductor chip (Spigarelli: column 9, lines 55-67; column 11, lines 1-10) and positioning said semiconductor chip on said substrate based on said patterns (Spigarelli: column 9, lines 45-65), and attaching said semiconductor chip to said mounting position on said substrate (Spigarelli: column 15, lines 45-67; column 16, lines 1-55), as in claim 7.

Regarding claim 9, Spigarelli discloses wherein said visible light includes light of a wavelength of 660 to 760 nm (Spigarelli: column 16, lines 35-67; column 17, lines 1-55), as in the claim.

Regarding claim 10, Spigarelli discloses wherein said semiconductor chip conveying means clamps and holds said semiconductor chip at a plurality of locations (Spigarelli: column 10, lines 28-37), as in the claim.

Regarding claim 11, Spigarelli discloses wherein said semiconductor chip conveying means is provided with at least one transparent part and clamps and holds said semiconductor chip at its entire surface other than said transparent parts (Spigarelli: column 11, lines 20-50), as in the claim.

Regarding claim 12, Spigarelli discloses wherein said semiconductor chip conveying means has a transparent part through which visible light passes up to the held semiconductor chip (Spigarelli: column 11, lines 20-50), as in the claim.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 2 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Spigarelli et al., (hereinafter referred to as "Spigarelli").

Spigarelli discloses semiconductor chip mounting apparatus for mounting a semiconductor chip on a substrate by flip-chip bonding (Spigarelli: figure 2), comprising: a stage on which the substrate is carried (Spigarelli: column 8, lines 45-55), a visible light source for directly illuminating the substrate from above the stage (Spigarelli: column 12, lines 50-67), a semiconductor chip conveying means for holding from one surface said semiconductor chip comprised of silicon formed to a thickness through which visible light can pass and conveying it on said substrate carried on the stage (Spigarelli: column 10, lines 15-45), a capturing means arranged at a position facing said stage and capturing visible light passing through said semiconductor chip held by said semiconductor chip conveying means so as to capture patterns formed on the substrate carried on said stage and said semiconductor chip (Spigarelli: column 9, lines 55-67; column 11, lines 1-10), and a positioning means for positioning said semiconductor chip on said substrate based on the patterns of said substrate and said semiconductor chip captured by said capturing means (Spigarelli: column 9, lines 45-65), as in claim 2. However, Spigarelli fails disclose that the thickness of the semiconductor chip is 5 to 20 μm, as in the claims. But Spigarelli does disclose that chip thickness (Spigarelli: column 1, lines 20-30) is a

consideration for chip placement (Spigarelli: column 14, lines 1-15). As such, the Examiner notes that it would have been obvious to one of ordinary skill in the art to restrict the chip thickness to the specified range of 5 to 20 μm in order to reduce the possibility of misalignment along the z-axis. The Spigarelli apparatus as operative upon chips with a thickness of 5 to 20 μm has all of the features of claim 2.

Spigarelli discloses semiconductor chip mounting method for mounting a semiconductor chip on a substrate by flip-chip bonding (Spigarelli: column 26, lines 1-43) including the steps of: holding a semiconductor chip comprised of silicon formed to a thickness passing visible light by a semiconductor chip conveying means from one surface and conveying it on a substrate carried on a stage (Spigarelli: column 10, lines 15-45), directly illuminating said substrate with visible light from above the stage (Spigarelli: column 12, lines 50-67), capturing visible light passing through said semiconductor chip by a capturing means arranged at a position facing said stage and thereby capturing patterns formed by said substrate and said semiconductor chip (Spigarelli: column 9, lines 55-67; column 11, lines 1-10) and positioning said semiconductor chip on said substrate based on said patterns (Spigarelli: column 9, lines 45-65), and attaching said semiconductor chip to said mounting position on said substrate (Spigarelli: column 15, lines 45-67; column 16, lines 1-55), as in claim 8. However, Spigarelli fails disclose that the thickness of the semiconductor chip is 5 to 20 μm, as in the claims. But Spigarelli does disclose that chip thickness (Spigarelli: column 1, lines 20-30) is a consideration for chip placement (Spigarelli: column 14, lines 1-15). As such, the Examiner notes that it would have been obvious to one of ordinary skill in the art to restrict the chip thickness to the specified range of 5 to 20 μm in order

to reduce the possibility of misalignment along the z-axis. The Spigarelli method as operative upon chips with a thickness of 5 to 20 μm has all of the features of claim 8.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Biggs discloses an angled wire bonding tool and alignment method. Distefano discloses a microelectronics unit mounting with multiple lead bonding.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andy S. Rao whose telephone number is (571)-272-7337. The examiner can normally be reached on Monday-Friday 8 hours.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mehrdad Dastouri can be reached on (571)-272-7418. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Andy S. Rao
Primary Examiner
Art Unit 2621

ANDY RAO
PRIMARY EXAMINER

asr
April 24, 2006